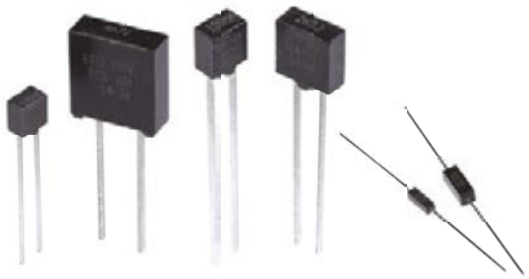
High Temperature Molded Capacitors

TCE / TCN Molded Series HT



FEATURES

- Multilayer chips ceramic capacitors for operating temperature up to 220°C
- NP0 and X7R dielectrics
- Capacitance range: 1pF to 10µF
- Voltage range at 20°C: 16 V_{DC} to 100 V_{DC}

PHYSICAL CHARACTERISTICS

CONSTRUCTION

Epoxy molded radial or axial leaded chips capacitors for through-hole circuits.

MARKING (clear or coded)

Series, capacitance value, tolerance, voltage, date code.

ELECTRICAL SPECIFICATIONS

Description	NP0	X7R
Operating temperature	–55°C to +220°C	–55°C to +220°C
Rated voltage at 20° C	16 V_{DC} to 100 V_{DC}	16 V_{DC} to 500 V_{DC}
Dielectric withstanding voltage at 20° C	2.5 U_{RC} for U_{RC} < 500 V_{DC} 1.5 U_{RC} for U_{RC} = 500 V_{DC}	2.5 U_{RC} for U_{RC} < 500 V_{DC} 1.5 U_{RC} for U_{RC} = 500 V_{DC}
Capacitance	at 1MHz for C ≤ 1,000pF at 1kHz for C > 1,000pF	at 1MHz for C ≤ 100pF at 1kHz for C > 100pF
Dissipation factor at 20° C	≤ 0.015 (150/C + 7)% at 1MHz for C ≤ 50pF ≤0.15% at 1MHz for 50pF < C ≤ 1,000pF ≤0.15% at 1kHz for C > 1,000pF	≤2.5% at 1MHz for C ≤ 100pF ≤2.5% at 1kHz for C > 100pF
Dissipation factor at 200° C	≤ 0.03 (150/C + 7)% at 1MHz for C ≤ 50pF ≤0.3% at 1MHz for 50pF < C ≤ 1,000pF ≤0.3% at 1kHz for C > 1,000pF	≤1.5% at 1MHz for C ≤ 100pF ≤1.5% at 1kHz for C > 100pF
Dissipation factor at 220° C	≤ 0.03 (150/C + 7)% at 1MHz for C ≤ 50pF ≤0.3% at 1MHz for 50pF < C ≤ 1,000pF ≤0.3% at 1kHz for C > 1,000pF	≤0.5% at 1MHz for C ≤ 100pF ≤0.5% at 1kHz for C > 100pF
Insulation resistance at 20° C under U_{RC}	≥ 50,000MΩ or ≥ 1,000MΩ.µF (whichever is less)	≥ 20,000MΩ or ≥ 500MΩ.µF (whichever is less)
Insulation resistance at 200° C under U_{RC}	≥ 1,000MΩ or ≥ 20MΩ.µF (whichever is less)	≥ 200MΩ or ≥ 5MΩ.µF (whichever is less)
Insulation resistance at 220° C under U_{RC}	≥ 200MΩ or ≥ 5MΩ.µF (whichever is less)	≥ 100MΩ or ≥ 2MΩ.µF (whichever is less)
Ageing	None	≤ 2.5% per decade hour

HOW TO ORDER

TCE 2 01 TCE 2X 01	-	W	12nF	10%	16 V
Series	Exxelia size code	Terminations	RoHS compliant	Capacitance	Tolerance	Rated voltage at 20° C

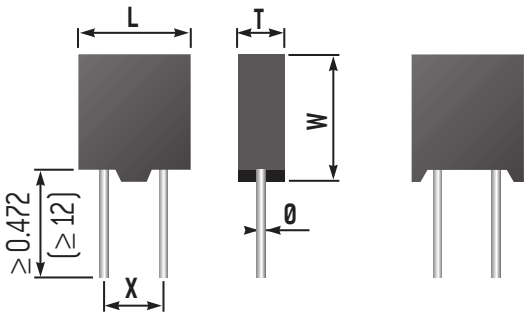
Operating temperature **Up to 200° C** **TCE2** = NP0 **TCN2** = X7R **Up to 220° C** **TCE2X** = NP0 **TCN2X** = X7R	**01** **02** **03** **04** **51** **52** **53** **54** **55** **56**	**-** = Tinned copper leads Available on sizes 01, 02, 03, 04: **D** = Tinned nickel leads	**-** = No RoHS **W** = RoHS compliant	Capacitance value in clear	NP0: cap. value ≤ 12pF **±0.25pF** cap. value ≤ 8.2pF **±0.5pF** **±1pF** cap. value > 22pF **±1%** cap. value > 12pF **±2%** cap. value > 8.2pF **±5%** **±10%** cap. value > 3.9pF **±20%**	X7R: **±10%** **±20%**	**16V** **25 V** **50 V** **100 V**

HIGH TEMPERATURE

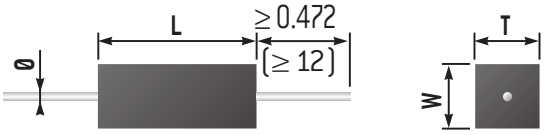
TCE / TCN Molded Series HT

High Temperature Molded Capacitors

DIMENSIONS in inches (mm)



TCE/TCN 201, 202, 203, 204



TCE/TCN 251, 252, 253, 254

STANDARD RATINGS

Exxelia size code			01		02		03		04		52		53		54	
Dimensions inches (mm)	L ± 0.02 (± 0.5)		0.122 (3.1)		0.197 (5)		0.295 (7.5)		0.394 (10)		0.217 (5.5)		0.295 (7.5)		0.394 (10)	
	W max.		0.178 (4.5)		0.237 (6)		0.335 (8.5)		0.434 (11)		0.099 (2.5)		0.099 (2.5)		0.154 (3.9)	
	T ± 0.008 (± 0.2)		0.098 (2.5)		0.098 (2.5)		0.098 (2.5)		0.138 (3.5)		0.098 (2.5)		0.098 (2.5)		0.154 (3.9)	
	X ± 0.008 (± 0.2)		0.1 (2.54)		0.1 (2.54)		0.2 (5.08)		0.2 (5.08)		-		-		-	
	Ø ± 10%		0.024 (0.6)		0.024 (0.6)		0.024 (0.6)		0.031 **(0.8)**		0.024 (0.6)		0.024 (0.6)		0.024 (0.6)	
Dielectric			NP0	X7R	NP0	X7R	NP0	X7R	NP0	X7R	NP0	X7R	NP0	X7R	NP0	X7R
Min. capacitance value			1pF	10pF	10pF	180pF	100pF	1.2nF	390pF	4.7nF	1pF	10pF	1pF	100pF	10pF	180pF
Rated voltage (U_{RC})	20°C	200°C	220°C													
	16V	8V	5V	12nF	470nF	56nF	2.2µF	180nF	10µF	330nF	10µF	12nF	470nF	22nF	1.2µF	56nF	2.2µF
	25V	12V	8V	6.8nF	220nF	39nF	1µF	82nF	4.7µF	180nF	4.7µF	6.8nF	220nF	15nF	680nF	39nF	1µF
	50V	25V	16V	3.3nF	120nF	18nF	560nF	56nF	2.7µF	120nF	2.7µF	3.3nF	120nF	8.2nF	270nF	18nF	560nF
	100V	50V	25V	1.5nF	39nF	8.2nF	220nF	33nF	1µF	56nF	1.5µF	1.5nF	39nF	3.9nF	120nF	8.2nF	220nF

Available capacitance values:
NP0: E6, E12, E24 (see page 14). Specific values upon request.
X7R: E6, E12 (see page 14). Specific values upon request.
The above table defines the standard products, other components may be built upon request.

General Information

High temperature capacitors are made of class 1 or class 2 ceramic dielectrics featuring special compositions based upon high purity oxides to reduce ionic conduction inherent to the presence of atoms such as sodium.

In addition, all quality controls carried out at intermediate and final production stages (lot acceptance test under U_{RC} and insulation resistance measurement at operating temperature) are the assurance of enhanced reliability.

High temperature capacitors include :

- chip class 1 (CEC 203 to CEC 233) and class 2 (CNC 203 to 233),
- encapsulated radial leads class 1 and 2 (TCE / TCN 201 to 204),
- encapsulated axial leads class 1 and 2 (TCE / TCN 252 to 254),
- selfprotected radial leads class 1 and 2 (TCE / TCN 212 to 216) and radial leads class 1 and 2 (TCE / TCN 263).

Mechanical stress is eliminated with replacement of epoxy by selfprotected ceramic. This also allows the increase of the capacitance ranges and improves the reliability.

- high voltage varnished capacitors (TCH 279 to 285)
- high capacitance value SCT Series.

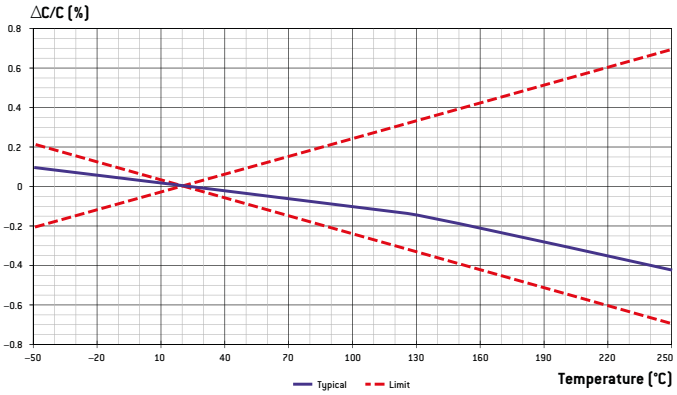
They are highly recommended for operation at temperatures of up to 200°C. Capacitors specifically designed for higher operating temperatures (e.g. TCE / TCN 212 to 216 and TCE / TCN 263 to 266) are also available.

High temperature capacitors are made of class 1 or class 2 ceramic dielectrics featuring special compositions based upon high purity oxides to reduce ionic conduction inherent to the presence of atoms such as sodium.

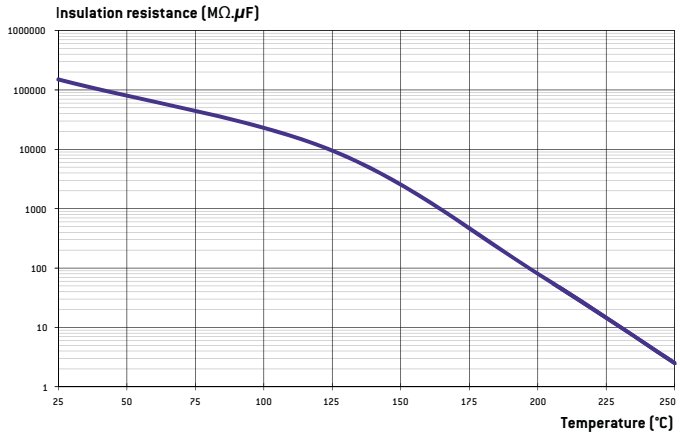
In addition, all quality controls carried out at intermediate and final production stages (lot acceptance test under 0.5 U_{RC} and insulation resistance measurement at 200°C) are the assurance of enhanced reliability.

TYPICAL CURVES: CE / CN Series, TCE / TCN Series, TCH Series

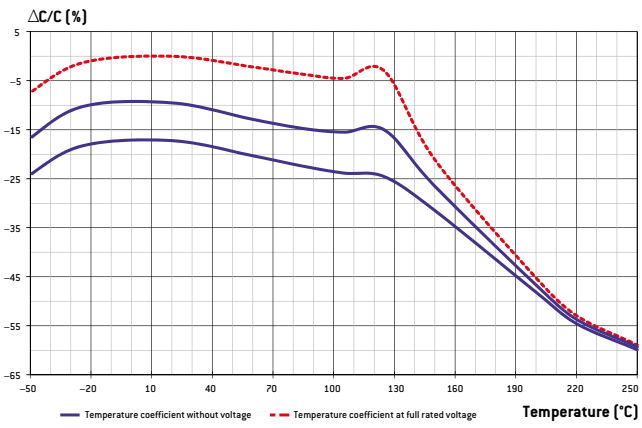
NPO: TYPICAL CAPACITANCE VARIATION VERSUS TEMPERATURE



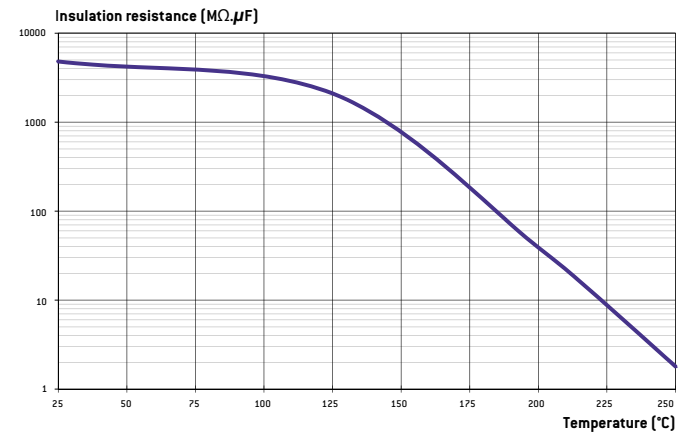
NPO: TYPICAL INSULATION RESISTANCE VERSUS TEMPERATURE



X7R: TYPICAL CAPACITANCE VARIATION VERSUS TEMPERATURE

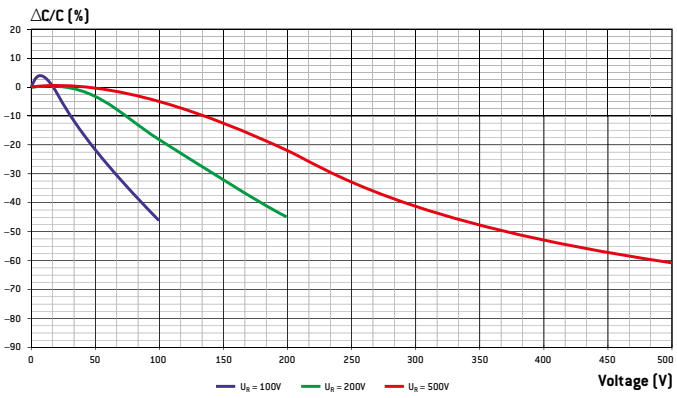


X7R: TYPICAL INSULATION RESISTANCE VERSUS TEMPERATURE

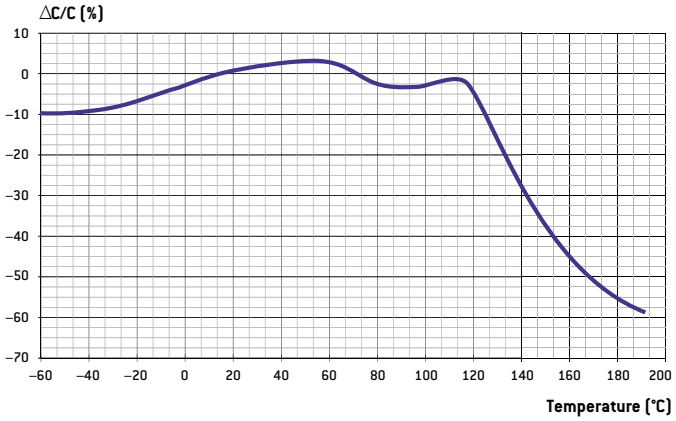


TYPICAL CURVES: SCT Series

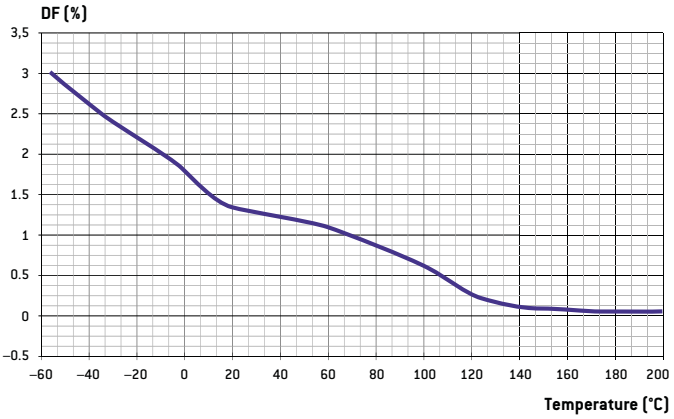
ΔC/C VERSUS APPLIED VOLTAGE AND RATED VOLTAGE (U_R)



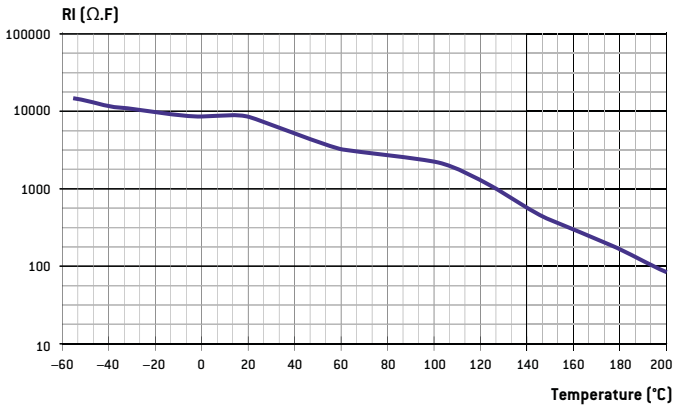
CAPACITANCE VERSUS TEMPERATURE



DIELECTRIC LOSSES VERSUS TEMPERATURE

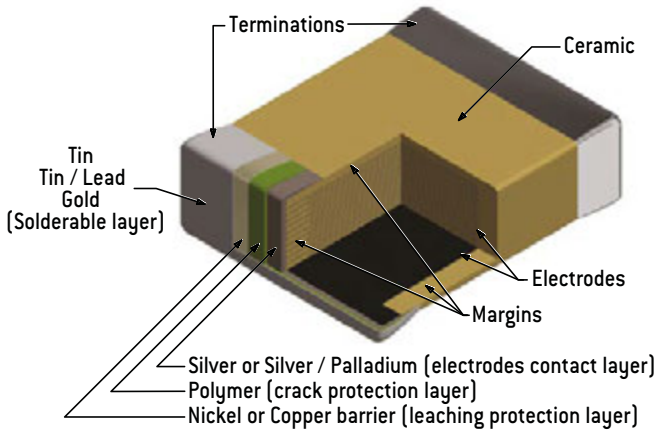


INSULATION RESISTANCE VERSUS TEMPERATURE



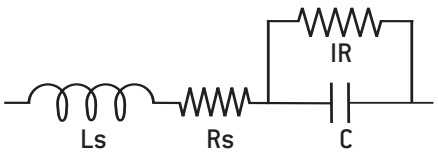
Ceramic Capacitors Technology

MLCC STRUCTURE



EQUIVALENT CIRCUIT

Capacitor is a complex component combining resistive, inductive and capacitive phenomena. A simplified schematic for the equivalent circuit is:



DIELECTRIC CHARACTERISTICS

Insulation Resistance (IR) is the resistance measured under DC voltage across the terminals of the capacitor and consists principally of the parallel resistance shown in the equivalent circuit. As capacitance values and hence the area of dielectric increases, the IR decreases and hence the product (C x IR) is often specified in Ω.F or MΩ.μF.

The Equivalent Series Resistance (ESR) is the sum of the resistive terms which generate heating when capacitor is used under AC voltage at a given frequency (f).

Dissipation factor (DF) is the ration of the apparent power input will turn to heat in the capacitor:

$$DF = 2\pi f C ESR$$

When a capacitor works under AC voltage, **heat power loss (P),** expressed in Watt, is equal to:

$$P = 2\pi f C Vrms^2 DF$$

The series inductance (Ls) is due to the currents running through the electrodes. It can distort the operation of the capacitor at high frequency where the **impedance (Z)** is given as:

$$Z = Rs + j(Ls.\omega - 1/(C.\omega)) \text{ with } \omega = 2\pi f$$

When frequency rises, the capacitive component of capacitors is gradually canceled up to the resonance frequency, where :

$$Z = Rs \text{ and } LsC.\omega^2 = 1$$

Above this frequency the capacitor behaves like an inductor.

	P100	NP0	N2200 (C4xx)	BX	2C1	X7R
Dielectric material	Porcelain	Magnesium titanate or Neodynium baryum titanate	Barium zirconate titanate	Baryum titanate ($BaTiO_3$)		
Dielectric constant	15 – 18	20 – 85	450	2,000 – 5,000		
Electrode technology	PME (Precious Metal Electrodes): Ag/Pd					
Capacitance variation between –-55°C and +125/° C without DC voltage	(100±30)ppm/° C	(0±30)ppm/° C	(–2,200±500) ppm/° C	±15%	±20%	±15%
Capacitance variation between –-55°C and +125/° C with DC rated voltage			0 -15%	15% –25%	20% –30%	Not applicable
Piezo-electric effect	None		None	Yes		
Dielectric absorption	None		Few %	Few %		
Thermal shock sensitive	+		+	++		

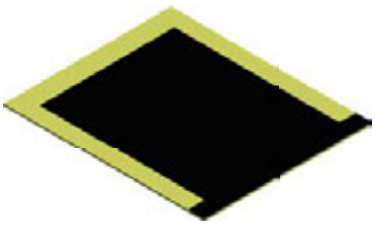
Ceramic Capacitors Technology

MANUFACTURING STEPS

SLIP CASTING

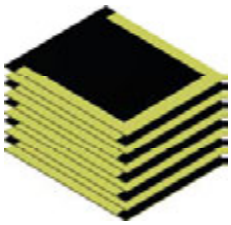
A slurry, a mix of ceramic powder, binder and solvents, is poured onto conveyor belt inside a drying oven, resulting in a dry ceramic sheet.

ELECTRODE SCREEN PRINTING



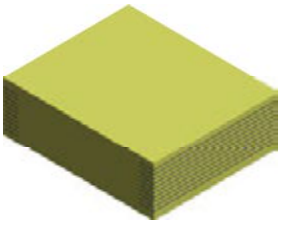
The electrode ink, made from a metal powder mixed with solvents, is printed onto the ceramic sheets using a screen printing process.

STACKING



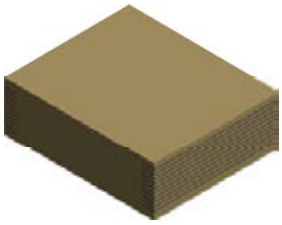
The sheets with electrode printed are stacked to create a multilayer structure.

PRESSING



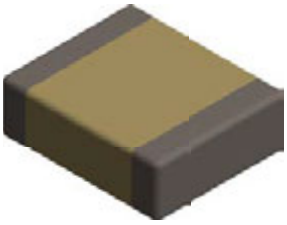
Pressure is applied to the stack to fuse all the separate layers, this created a monolithic structure.

SINTERING



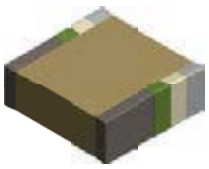
The parts are sintered in an oven with a precise temperature profile which is very important to the characteristics of the capacitors.

TERMINATIONS



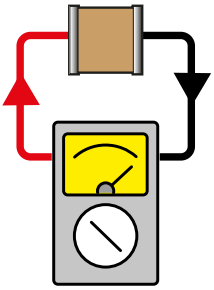
Each terminal of the capacitor is dipped in the termination ink, mix of metal powder, solvents and glass frit and the parts are fired in an oven.

TERMINATIONS PLATING



Stacking + leads soldering + encapsulation
(see pages 10-11)

FINAL TESTING



PACKAGING

User Guide

SMD TERMINATIONS

NON RoHS COMPLIANT	Code	RoHS COMPLIANT	Code	Magnetic	Recommended mounting process						Storage (months)*
					Epoxy bonding	Iron soldering	Wave soldering	Vapor phase soldering	Infrared soldering	Wire bonding	
Ag	**Q**	Ag	**QW / P**	No	●	●	●	●			18
Ag/Pd/Pt	**-**	Ag/Pd/Pt	**W / A**	No	●	●	●				24
Ag + Ni + dipped Sn/Pb 60/40	**T****	-	**-**	No		●	●	●	●		24
Ag/Pd/Pt + dipped Sn/Pb 60/40	**H**	Ag/Pd/Pt + dipped Sn	**HW**	No		●					24
Ag + Ni + electrolytic Sn/Pb 95/5	**C**	Ag + Ni + electrolytic Sn	**CW / S**	Yes		●	●	●	●		18
Ag + Ni + electrolytic Sn/Pb 60/40	**D**	-	**-**	Yes		●	●	●	●		18
-	**-**	Ag + Cu + electrolytic Sn	**C*****	No		●	●	●	●		18
Ag + Ni + dipped Sn/Pb 60/40	**E**	Ag + Ni + electrolytic Sn	**EW**	Yes		●	●				24
Ag + Ni + Au	**G**	Ag + Ni + Au	**GW**	Yes	●	●	●	●	●	●	36
Ag + Polymer + Ni + Sn/Pb 95/5	**YC**	Ag + Polymer + Ni + Sn	**YCW**	Yes		●	●	●	●		18
Ag + Polymer + Ni + Sn/Pb 60/40	**YD**	-	**-**	Yes		●	●	●	●		18
Ag + Polymer + Ni + Au	**YG**	Ag + Polymer + Ni + Au	**YGW**	Yes	●	●	●	●	●	●	36

Nickel (Ni) or Copper (Cu) barriers amplify thermal shock and are not recommended for chip sizes larger than 3030.

* Storage must be in a dry environment at a temperature of 20° C with a relative humidity below 50%, or preferably in a package enclosing a desiccant.
** Maintenance only.
*** Non magnetic chips series only.

SMD ENVIRONMENTAL TESTS

Ceramic chip capacitors for SMD are designed to meet test requirements of **CECC 32100** and **NF C 93133** standards as specified below in compliance with NF C 20700 and IEC 68 standards:

- Solderability: **NF C 20758,** 260° C, bath 62/36/2.
- Adherence: 5N force.
- Vibration fatigue test: **NF C 20706,** 20 g, 10 Hz to 2,000 Hz, 12 cycles of 20 minutes each.
- Rapid temperature change: **NF C 20714,** – –55°C to + 125° C, 5 cycles.
- Combined climatic test: **IEC 68-2-38.**
- Damp heat: **NF C 20703,** 93 %, H.R., 40° C.
- Endurance test: 1,000 hours, 1.5 U_{RC}, 125° C.

STORAGE OF CHIP CAPACITORS

TINNED OR NON TINNED CHIP CAPACITORS

Storage must be in a dry environment at a temperature of 20°C with a relative humidity below 50 %, or preferably in a packaging enclosing a desiccant.

STORAGE IN INDUSTRIAL ENVIRONMENT:

- 2 years for tin dipped chip capacitors,
- 18 months for tin electroplated chip capacitors,
- 2 years for non tinned chip capacitors,
- 3 years for gold plated chip capacitors.

STORAGE IN CONTROLLED NEUTRAL NITROGEN ENVIRONMENT:

- 4 years for tin dipped or electroplated chip capacitors,
- 4 years for non tinned chip capacitors,
- 5 years for gold plated chip capacitors.

Storage duration should be considered from delivery date and not from batch manufacture date. The tests carried out at final acceptance stage (solderability, susceptibility to solder heat) enable to assess the compatibility to surface mounting of the chips.

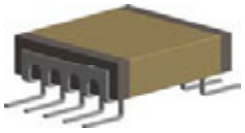
LEAD STYLES

SURFACE MOUNTING

DIL LEADS

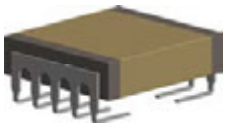
P style

PL style



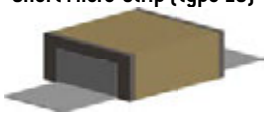
L style

J style

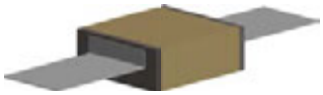


RIBBON LEADS

Micro-strip (type 1)
Short Micro-strip (type 1S)

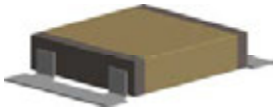


Axial (Type 2)

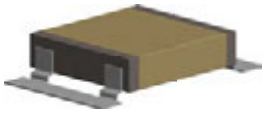


Radial (Type 3)

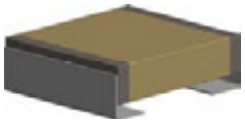
R style



RX style



RJ style



Please contact Exxelia sales for any lead configuration not shown.

TROUGH-HOLE MOUNTING

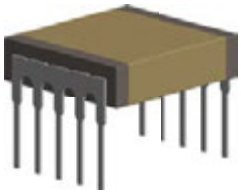
AXIAL AND RADIAL

Radial leads (Type 6)

Radial leads (4 leads)

Axial leads (Type 7)

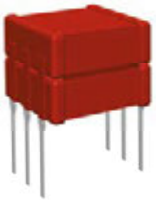
DIL leads: N style



ENCAPSULATION STYLES

Ceramic encapsulation
(selfprotected)

Varnish



Conformal coating

Molding

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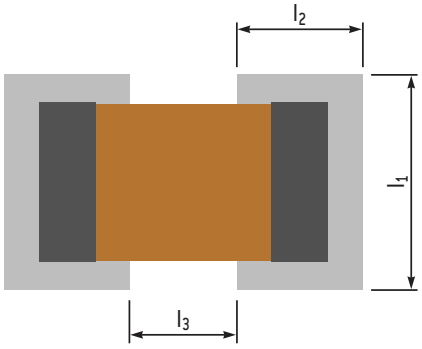
SOLDERING ADVICES FOR REFLOW SOLDERING



Large chips above size 2225 are not recommended to be mounted on epoxy board due to thermal expansion coefficient mismatch between ceramic capacitor and epoxy. Where larger sizes are required, it is recommended to use components with ribbon or other adapted leads so as to absorb thermo-mechanical strains.

Dimensions in inches (in mm)	Reflow soldering						Wave soldering					
	I_1		I_2		I_3		I_1		I_2		I_3	
0402	0.043	(1.1)	0.035	(0.9)	0.012	(0.3)	0.043	(1.1)	0.047	(1.2)	0.012	(0.3)
0403	0.055	(1.4)	0.035	(0.9)	0.012	(0.3)	0.055	(1.4)	0.047	(1.2)	0.012	(0.3)
0504	0.063	(1.6)	0.051	(1.3)	0.016	(0.4)	0.063	(1.6)	0.063	(1.6)	0.016	(0.4)
0603	0.055	(1.4)	0.059	(1.5)	0.02	(0.5)	0.055	(1.4)	0.071	(1.8)	0.02	(0.5)
0805	0.073	(1.85)	0.065	(1.65)	0.024	(0.6)	0.073	(1.85)	0.077	(1.95)	0.024	(0.6)
0907	0.094	(2.4)	0.065	(1.65)	0.035	(0.9)	0.094	(2.4)	0.077	(1.95)	0.035	(0.9)
1005	0.073	(1.85)	0.067	(1.7)	0.039	(1)	0.073	(1.85)	0.079	(2)	0.039	(1)
1206	0.083	(2.1)	0.067	(1.7)	0.059	(1.5)	0.083	(2.1)	0.079	(2)	0.059	(1.5)
1210	0.118	(3)	0.069	(1.75)	0.059	(1.5)	0.118	(3)	0.081	(2.05)	0.059	(1.5)
1605	0.073	(1.85)	0.071	(1.8)	0.087	(2.2)	0.073	(1.85)	0.083	(2.1)	0.087	(2.2)
1806	0.087	(2.2)	0.073	(1.85)	0.102	(2.6)	0.087	(2.2)	0.085	(2.15)	0.102	(2.6)
1812	0.152	(3.85)	0.073	(1.85)	0.102	(2.6)	0.152	(3.85)	0.085	(2.15)	0.102	(2.6)
1825	0.281	(7.15)	0.073	(1.85)	0.102	(2.6)	0.281	(7.15)	0.085	(2.15)	0.102	(2.6)
2210	0.13	(3.3)	0.079	(2)	0.146	(3.7)	0.13	(3.3)	0.091	(2.3)	0.146	(3.7)
2220	0.228	(5.8)	0.079	(2)	0.146	(3.7)	0.228	(5.8)	0.091	(2.3)	0.146	(3.7)
2225	0.281	(7.15)	0.079	(2)	0.146	(3.7)	0.281	(7.15)	0.091	(2.3)	0.146	(3.7)

RECOMMENDED FOOTPRINT FOR SMD CAPACITORS

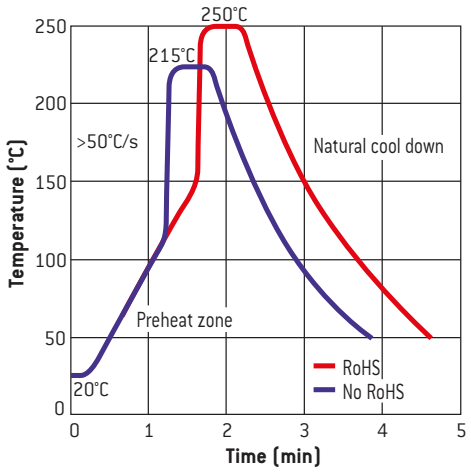
Ceramic is by nature a material which is sensitive both thermally and mechanically. Stresses caused by the physical and thermal properties of the capacitors, substrates and solders are attenuated by the leads.

Wave soldering is unsuitable for sizes larger than 2220 and for the higher ends of capacitance ranges due to possible thermal shock (capacitance values given upon request).

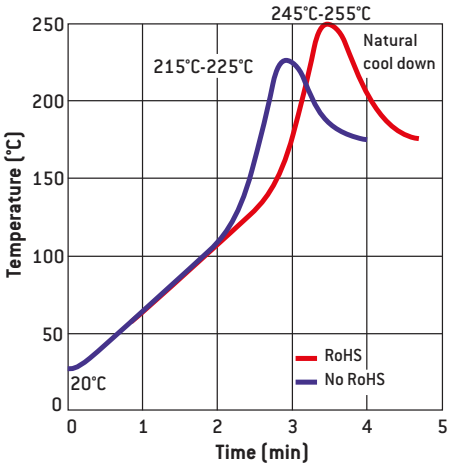
Infrared and vapor phase reflow, are preferred for high reliability applications as inherent thermo-mechanical strains are lower than those inherent to wave soldering.

Whatever the soldering process is, it is highly recommended to apply a thermal cycle, see hereafter our recommended soldering profile:

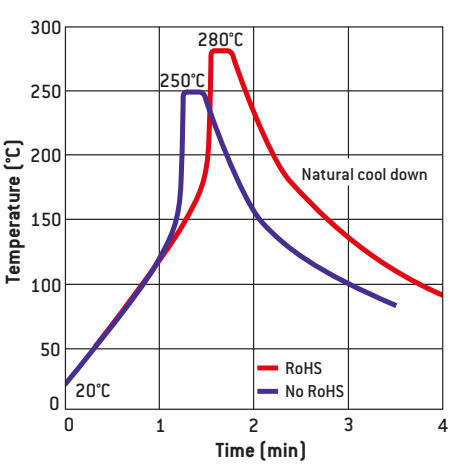
RECOMMENDED VAPOR PHASE REFLOW PROFILE



RECOMMENDED IR REFLOW PROFIL



RECOMMENDED WAVE SOLDERING PROFILE



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SOLDERING ADVICES FOR IRON SOLDERING

Attachment with a soldering iron is discouraged due to ceramic brittleness and the process control limitations. In the event that a soldering iron must be used, the following precautions should be observed:

- Use a substrate with chip footprints big enough to allow putting side by side one end of the capacitor and the iron tip without any contact between this tip and the component,
- place the capacitor on this footprint,
- heat the substrate until the capacitor's temperature reaches 150° C minimum (preheating step, maximum 1°C per second),
- place the hot iron tip (a flat tip is preferred) on the footprint **without touching the capacitor.** Use a regulated iron with a 30 watts maximum power. The recommended temperature of the iron is 270 ±10° C. The temperature gap between the capacitor and the iron tip must not exceed 120° C,
- leave the tip on the footprint for a few seconds in order to increase locally the footprint's temperature,
- use a cored wire solder and put it down on the iron tip. In a preferred way use Sn/Pb/Ag 62/36/2 alloy,
- wait until the solder fillet is formed on the capacitor's termination,
- take away iron and wire solder,
- wait a few minutes so that the substrate and capacitor come back down to the preheating temperature,
- solder the second termination using the same procedure as the first,
- let the soldered component cool down slowly to avoid any thermal shock.

PACKAGING

TAPE AND REEL

The films used on the reels correspond to standard IEC 60286-3. Films are delivered on reels in compliance with document IEC 286-3 dated 1991.

Minimum quantity is 250 chips.

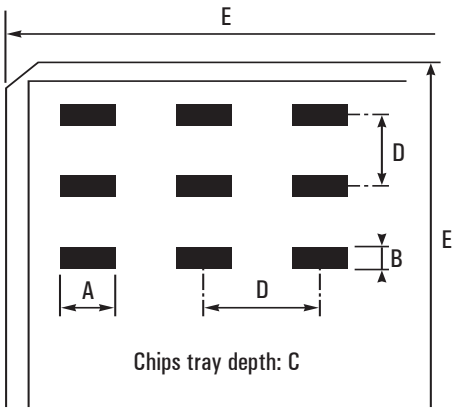
Maximum quantities per reel are as follows:

- Super 8 reel - Ø 180: 2,500 chips.
- Super 8 reel - Ø 330: 10,000 chips.
- Super 12 reel - Ø 180: 1,000 chips.

Reel marking complies with CECC 32100 standard:

- Model.
- Rated capacitance.
- Capacitance tolerance.
- Rated voltage.
- Batch number.

TRAY PACKAGES



DIMENSIONAL CHARACTERISTICS OF CHIPS TRAY PACKAGES

Sizes	Nr. of chips/ package	Oriented chips	Dimensions in inches (in mm)				
			A	B	C	D	E
0402	100	No	Ø 0.112 (Ø 3.02)		0.065 (1.65)	0.167 (4.24)	2 (50.8)
0403	100	No	Ø 0.112 (Ø 3.02)		0.065 (1.65)	0.167 (4.24)	2 (50.8)
0504	100	Yes	0.059 (1.5)	0.045 (1.14)	0.035 (0.89)	0.167 (4.24)	2 (50.8)
0603	340	Yes	0.1 (2.54)	0.06 (1.52)	0.045 (1.14)	0.167 (4.24)	2 (50.8)
0805	100	Yes	0.1 (2.54)	0.06 (1.52)	0.045 (1.14)	0.167 (4.24)	2 (50.8)
1206	100	No	0.14 (3.56)	0.14 (3.56)	0.06 (1.52)	0.167 (4.24)	2 (50.8)
1210	100	Yes	0.14 (3.56)	0.14 (3.56)	0.06 (1.52)	0.167 (4.24)	2 (50.8)
1812	100	No	0.25 (6.35)	0.25 (6.35)	0.13 (3.3)	0.345 (8.76)	4 (101.6)
	25	Yes	0.24 (6.1)	0.265 (6.73)	0.07 (1.78)	0.345 (8.76)	2 (50.8)
2220	100	Yes	0.25 (6.35)	0.25 (6.35)	0.13 (3.3)	0.345 (8.76)	4 (101.6)
	25	Yes	0.24 (6.1)	0.265 (6.73)	0.07 (1.78)	0.345 (8.76)	2 (50.8)

User Guide

EIA STANDARD CAPACITANCE VALUES

Following EIA standard, the values and multiples that are indicated in the chart below can be ordered. E48, E96 series and intermediary values are available upon request.

E6 (± 20%)	E12 (± 10%)	E24 (± 5%)
10	10	10
		11
	12	12
		13
15	15	15
		16
	18	18
		20
22	22	22
		24
	27	27
		30
33	33	33
		36
	39	39
		43
47	47	47
		51
	56	56
		62
68	68	68
		75
	82	82
		91

PART MARKING VOLTAGE CODES

Use the following voltage code chart for part markings:

Voltage (V)	Code	Letter code
25	250	A
40	400	B
50	500	C
63	630	D
100	101	E
200	201	G
250	251	H
400	401	K
500	501	L
1,000	102	M
2,000	202	P
3,000	302	R
4,000	402	S
5,000	502	T
7,500	752	U
10,000	103	W

EIA CAPACITANCE CODE

The capacitance is expressed in three digit codes and in units of pico Farads (pF). The first and second digits are significant figures of the capacitance value and the third digit identifies the multiplier.

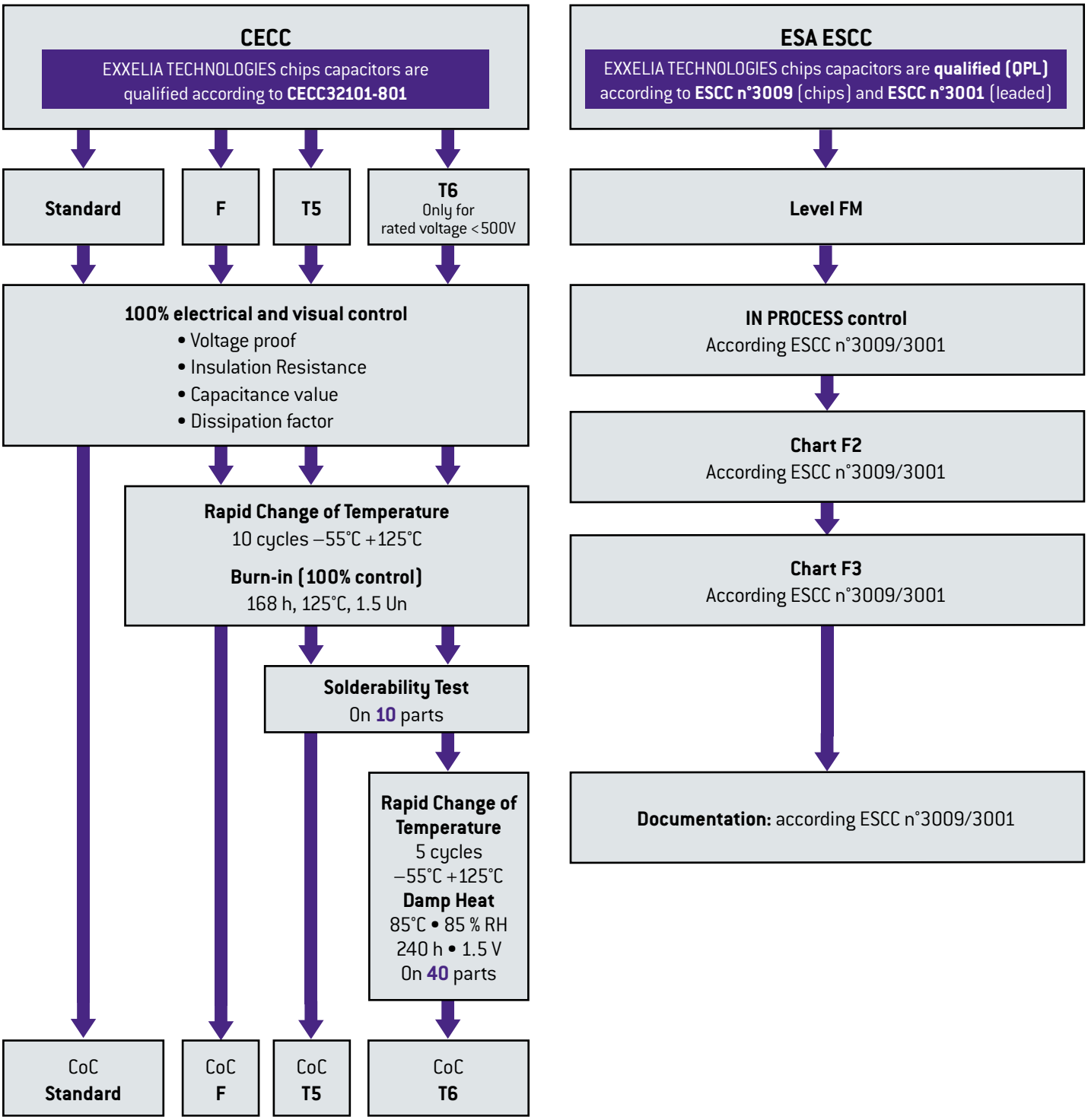
For capacitance value < 10pF, R designates a decimal point.
See examples below:

EIA code	Capacitance value		
	in pF	in nF	in µF
2R2	2.2	0.0022	0.0000022
6R8	6.8	0.0068	0.0000068
220	22	0.022	0.000022
470	47	0.047	0.000047
181	180	0.18	0.00018
221	220	0.22	0.00022
102	1,000	1	0.001
272	2,700	2.7	0.0027
123	12,000	12	0.012
683	68,000	68	0.068
124	120,000	120	0.12
564	560,000	560	0.56
335	3,300,000	3,300	3.3
825	8,200,000	8,200	8.2
156	15,000,000	15,000	15
686	68,000,000	68,000	68
107	100,000,000	100,000	100
227	220,000,000	220,000	220

PART MARKING TOLERANCE CODES

Use the following tolerance code chart for part markings:

Tolerance	Letter code
±0.25pF	CU
±0.5pF	DU
±1pF	FU
±1%	F
±2%	G
±5%	J
±10%	K
±20%	M

RELIABILITY LEVELS

Exxelia proposes different reliability levels for the ceramic capacitors for both NP0 and X7R ceramics.